FLEX-IMX8M-Mini SYSTEM ON MODULE PRODUCT MANUAL

(WITH NXP i.MX8M Mini SoC)

VER. 1.00

January 31, 2020

REVISION HISTORY

Revision	Date	Originator	Notes
0.1	November 6, 2019	TechNexion	Preliminary
1.00	January 31, 2020	TechNexion	General Public Release

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1. Introduction

1.1. General Introduction

The FLEX-IMX8M-Mini is a high performance highly integrated FLEX Compute Module designed around the NXP i.MX8M Mini Quad core ARM Cortex-A53 + Cortex-M4 applications processor. The FLEX-IMX8M-Mini provides an ideal building block that easily integrates with a wide range of target markets requiring compact, cost effective with low power consumption.

The modular approach offered by the FLEX Compute Module gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

2. FLEX-IMX8M-Mini Product Overview

The FLEX-IMX8M-Mini is a high performance, versatile System-on-Module in FLEX form factor optimized for audio, voice, video streaming applications.

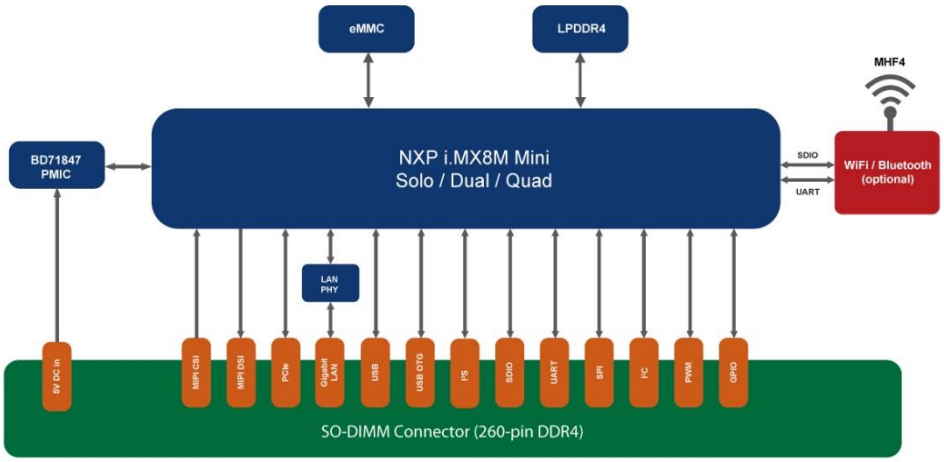
2.1. FLEX-IMX8M-Mini System-on-Module Overview

The FLEX-IMX8M-Mini System-on-Module has 3 Hirose high-speed 70 pin board-to-board connectors and integrates the NXP i.MX8M Mini, Memory, eMMC, Power Management IC (PMIC) and Wi-Fi / Bluetooth features.

Figure 1 – FLEX-IMX8M-Mini System-on-Module

2.2. Block Diagram

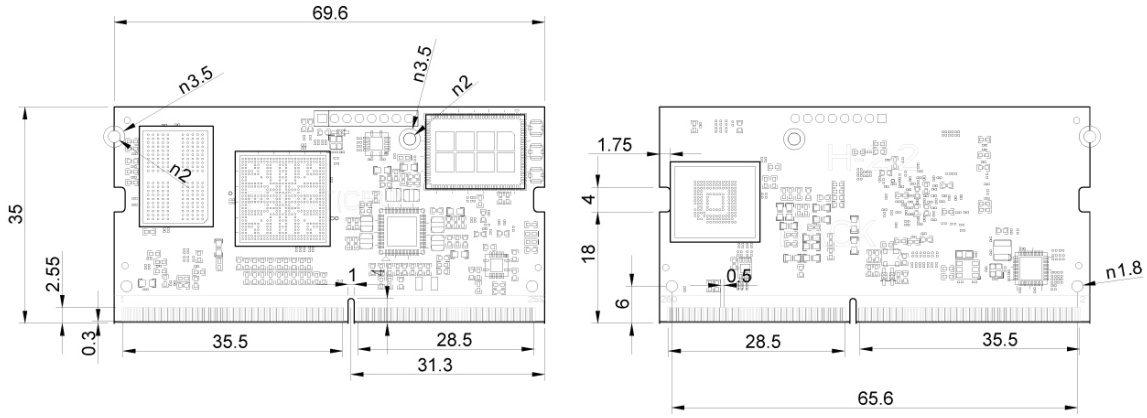
Figure 2 – FLEX-IMX8-Mini System-on-Module Block Diagram Overview



2.3. Dimensional Drawing

The FLEX-IMX8-Mini System-on-Module is an ultra-compact module in FLEX form factor.

Figure 3 – FLEX-IMX8-Mini System-on-Module Dimensions



2.4. Component Location

Figure 4 – FLEX-IMX8M-Mini Top View

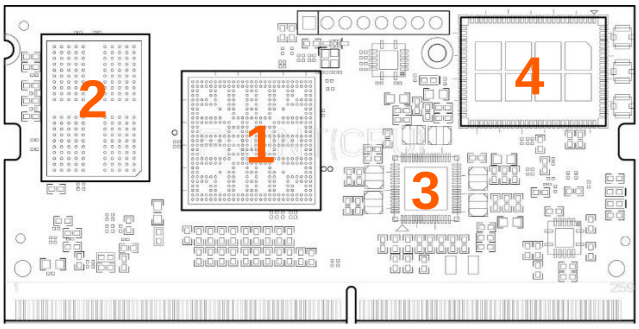
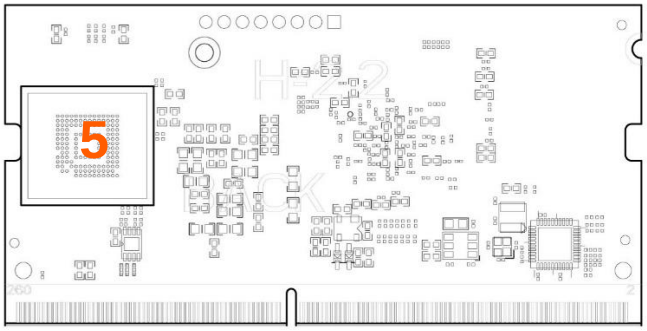


Figure 5 – FLEX-IMX8M-Mini Bottom View



No.	Description	No.	Description
1	NXP i.MX8M Mini Processor	4	Wi-Fi/Bluetooth Module (optional)
2	Memory IC	5	eMMC Storage IC
3	ROHM BD71847 PMIC		

3. Core Components

3.1. NXP i.MX8M Mini ARM Cortex-A53 + Cortex-M4 Processor

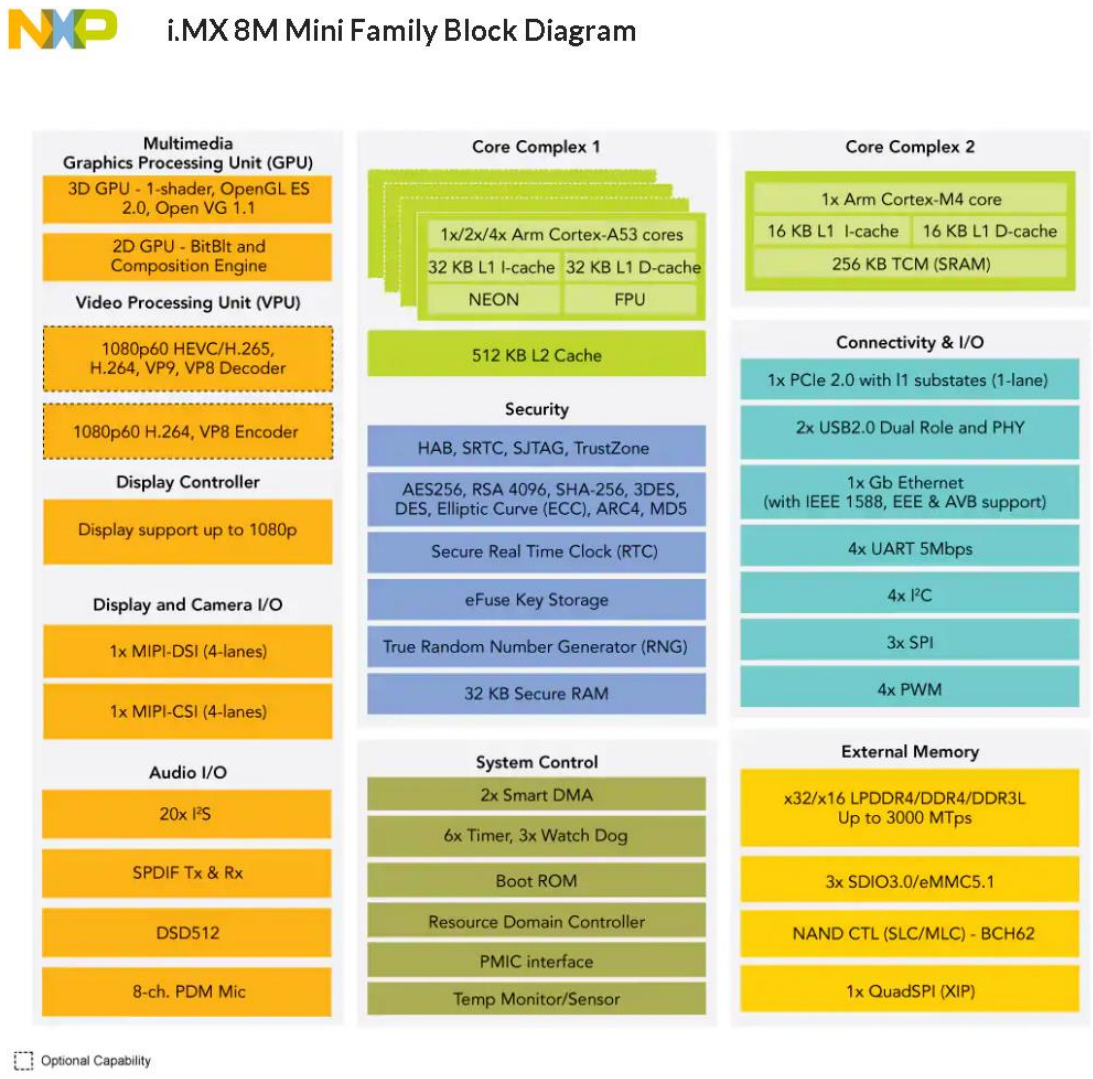
The i.MX 8M Mini is NXP's first embedded multicore applications processor built using advanced 14LPC FinFET process technology, providing more speed and improved power efficiency. With commercial and industrial level qualification and backed by NXP's product longevity program, the i.MX 8M Mini family may be used in any general purpose industrial and IoT application.

For additional details, please refer to the "i.MX8M Mini Applications Processor Reference Manual".

The i.MX8M Mini has the following features :

- Multicore Processing
  - 4x Cortex-A53 core platforms up to 1.8GHz per core
  - 32KB L1-I Cache/ 32 kB L1-D Cache
  - 512 kB L2 Cache
  - 1x Arm Cortex-M4 core up to 400MHz
  - 16 kB L1-I Cache/ 16 kB L2-D Cache
- GPU
  - 3D GPU (1x shader, OpenGL ES 2.0)
  - 2D GPU
- Display Interface
  - 1x MIPI DSI (4-lane) with PHY
- Video Playback
  - 1080p60 VP9 Profile 0, 2 (10-bit) decoder, HEVC/H.265 decoder, AVC/H.264 Baseline, Main, High decoder, VP8 decoder
  - 1080p60 AVC/H.264 encoder, VP8 encoder
- Audio
  - 5x SAI (12Tx + 16Rx external I2S lanes), 8ch PDM input
- Camera Interface
  - 1x MIPI CSI (4-lane) with PHY
- USB
  - 2x USB 2.0 OTG controllers with integrated PHY
- PCIe
  - 1x PCIe 2.0 (1-lane) with L1 low power sub states
- Ethernet
  - 1x Gigabit Ethernet (MAC) with AVB and IEEE 1588, Energy Efficient Ethernet (EEE) for low power
- Operating Systems
  - Linux, Android, FreeRTOS
- Temperature
  - Consumer (0°C to 95°C Tj)
  - Industrial (-40°C to 105°C Tj)
- Package
  - FCBGA, 14x14 0.5mm pitch

Figure 6 – NXP i.MX8M-Mini Processor Blocks



3.2. Power Management IC (ROHM BD71847)

The FLEX-IMX8M-Mini has an on onboard ROHM BD71847 power management integrated circuit (PMIC) that features a configurable architecture supporting the numerous outputs with various current ratings as well as programmable voltage and sequencing required by the components on the FLEX-IMX8M-Mini module.

Table 1 – PMIC Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	I/O	Description
E13	I2C4_SDA	I2C4_SDA	SDA	I/O	I2C bus data line
D13	I2C4_SCL	I2C4_SCL	SCL	I	I2C bus clock line
B24	POR_B	POR_B	POR_B	O	PMIC Reset Signal
A24	PMIC_ON_REQ	PMIC_ON_REQ	PMIC_ON_REQ	I	PMIC Power on request Input from processor (this signal has an external pull-up resistor)
E24	PMIC_STBY_REQ	PMIC_STBY_REQ	PMIC_STBY_REQ	I	PMIC Power standby request input from processor
K24	NAND_DATA01	GPIO3_IO07	IRQ_B	O	PMIC Interrupt Signal
F24	RTC_RESET_B	RTC_RESET_B	RTC_RESET_B	O	PMIC RTC Reset Signal
A26	RTC_XTALI	RTC_XTALI	C32K_OUT	O	32.768 KHz Clock
AG12	GPIO1_IO04	USDHC2_VSELECT	SD_VSELECT	O	SD Card Voltage Selection Signal (on module only)

3.2.1. ROHM BD71847 Reset Signal

To perform a hard-reset of the FLEX-IMX8M-Mini a software reset signal can be implemented. By connecting a Watchdog circuit on the carrier board by using PIN 238

Table 2 – PMIC Reset Signal Description

CPU BALL	CPU PAD NAME	Pinmux (mode)	Signal	V	I/O	Description
AG13	GPIO1_IO02	WDOG1_B	WDOG_B	3V3	I	Connected to the WDOG_B signal of PMIC and i.MX8M-Mini SoC

To perform a hard-reset of the FLEX-IMX8M-Mini an external circuit (for example a button or external watchdog IC) can be integrated on the carrier board by using PIN 238.

Table 3 – PMIC Hard Reset Signal Description

Connector	Signal	V	I/O	Description
9	PWRON_B	1V8	I	Connected to Reset Power Signal of PMIC

3.3. Memory

The FLEX-IMX8M-Mini integrates Low Power Double Data Rate IV (LPDDR4) Synchronous DRAM is connected over a 32-Bit dual channel configuration. (16 bit per channel).

The following memory chip manufacturers have been validated and tested on the FLEX-IMX8M-Mini Compute Module:

- SKHynix
- Kingston
- Micron
- Samsung
- ISSI

3.4. eMMC Storage

The FLEX-IMX8M-Mini can be ordered with onboard eMMC storage in different configurations and capacity. The onboard eMMC device is connected on the USDHC3 pins of the i.MX8M Mini processor in an 8-bit width configuration.

The following eMMC chip manufacturers have been validated and tested on the FLEX-IMX8M-Mini System-on-Module:

- Kingston eMMC
- Micron eMMC
- Sandisk iNAND

Table 4 – eMMC Signal Description

CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
M26	NAND_DATA04	USDHC3_DATA0	1V8	I/O	MMC/SDIO Data bit 0
L26	NAND_DATA05	USDHC3_DATA1	1V8	I/O	MMC/SDIO Data bit 1
K26	NAND_DATA06	USDHC3_DATA2	1V8	I/O	MMC/SDIO Data bit 2
N26	NAND_DATA07	USDHC3_DATA3	1V8	I/O	MMC/SDIO Data bit 3
N27	NAND_RE_B	USDHC3_DATA4	1V8	I/O	MMC/SDIO Data bit 4
M27	NAND_CE2_B	USDHC3_DATA5	1V8	I/O	MMC/SDIO Data bit 5
L27	NAND_CE3_B	USDHC3_DATA6	1V8	I/O	MMC/SDIO Data bit 6
K27	NAND_CLE	USDHC3_DATA7	1V8	I/O	MMC/SDIO Data bit 7
R27	NAND_WP_B	USDHC3_CMD	1V8	I/O	MMC/SDIO Command
R26	NAND_WE_B	USDHC3_CLK	1V8	O	MMC/SDIO Clock
P27	NAND_CE1_B	USDHC3_STROBE	1V8	O	This signal is generated by the device and used for output in HS400 Mode

3.5. Wi-Fi/Bluetooth

The FLEX-IMX8M-Mini has an optional pre-certified high-performance TechNexion PIXI-9377 dual band 2.4/5Ghz Wi-Fi / Bluetooth 5 Qualcomm Atheros QCA9377 based module on board.

The PIXI-9377 Wi-Fi / Bluetooth module is designed to operate with a single antenna for Wi-Fi and Bluetooth by using the MHF4 connector.

Key Features of the PIXI-9377 are:

- IEEE 802.11 ac/a/b/g/n 2.4 / 5Ghz
- Bluetooth 5
- MHF4 antenna connector
- Linux and Android drivers
- Wi-Fi / BT module board certifications with multiple antennas:
    - FCC (USA)
    - IC (Canada
    - ETSI (Europe)
    - Giteki / Telec (Japan)
    - RCM / C-tick (Australia / New Zealand).
- Industrial operation temperature range: -40°C to +85°C

The following pre-certified matching antennas are available with our distributors.

Partnumber	Description
ANTP180A138045D2450MHF4	4.5dBi dipole antenna
ANTP180A207070D2450MHF4	7dBi dipole antenna
ANTP150P232525D2450MHF4	2.5dBi PCB patch antenna

Figure 7 – FLEX-IMX8M-Mini Wi-Fi Module and Antenna Connector Location

Table 5 – Wi-Fi Signal Description

i.MX8M BALL	PAD NAME	Signal	I/O	Description
Y27	SD1_DATA0	USDHC1_DATA0	I/O	MMC/SDIO Data bit 0
Y26	SD1_DATA1	USDHC1_DATA1	I/O	MMC/SDIO Data bit 1
T27	SD1_DATA2	USDHC1_DATA2	I/O	MMC/SDIO Data bit 2
T26	SD1_DATA3	USDHC1_DATA3	I/O	MMC/SDIO Data bit 3
V27	SD1_CMD	USDHC1_CMD	I/O	MMC/SDIO Command
V26	SD1_CLK	USDHC1_CLK	O	MMC/SDIO Clock
N22	NAND_ALE	GPIO3_IO00 WL_HOST_WAKE	O	Host wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
AG14	GPIO1_IO00	GPIO1_IO00 WL_REG_ON	O	Wi-Fi device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Wi-Fi device must wake-up or remain awake. • Deserted: Wi-Fi device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

Table 6 – Bluetooth Signal Description

i.MX8M BALL	PAD NAME	Signal	I/O	Description
F13	UART1_TXD	UART1_TXD	O	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface
E14	UART1_RXD	UART1_RXD	I	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
E18	UART3_RXD	UART1_CTS	I/O	Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.
D18	UART3_TXD	UART1_RTS	I/O	Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.
AG15	SAI1_RXD0	SAI1_RXD0	I	Integrated Interchip Sound (I^2S) channel receive data line
AG20	SAI1_TXD0	SAI1_TXD0	O	Integrated Interchip Sound (I^2S) channel transmit data line
AC18	SAI1_TXC	SAI1_TXC	O	Integrated Interchip Sound (I^2S) channel word clock signal
AB19	SAI1_TXFS	SAI1_TXFS	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal
P26	NAND_READY_B	GPIO3_IO16 BT_HOST_WAKE	I	Host UART wake up. Signal from the module to the host indicating that the module requires Attention. • Asserted: Host device must wake-up or remain awake. • Deserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
AF13	GPIO1_IO03	GPIO1_IO03 BT_REG_ON	O	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention. • Asserted: Bluetooth device must wake-up or remain awake. • Deserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

3.6. Atheros AR8035 Gigabit LAN

The FLEX-IMX8M-Mini connects the i.MX8M Mini processor RGMII interface to the Atheros AR8035 gigabit Ethernet chip.

The AR8035 supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

Features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII and/or SGMII interfaces to MAC devices
- Supports Fibre and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000 BASE-X and 100 BASE-FX with Integrated SerDes
- RGMII timing modes support internal delay and external delay on Rx path
- Supports Atheros Green ETHOS® power saving modes with internal automatic DSP power saving scheme
- Supports IEEE 802.3az (Energy Efficient Ethernet) n Supports SmartEEE which allows MAC/ SoC devices without 802.3az support to function as the complete 802.3az system
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Multiple loopback modes for diagnostics
- Robust Surge Protection with ±750 V/ differential mode and ±4 kV/common mode
- Cable Diagnostic Test (CDT)

For more information, please contact your TechNexion sales representative.

Table 7 - Gigabit Ethernet interconnect between i.MX8M Mini and AR8035

CPU BALL	PAD NAME	Signal	AR8035 PIN	Description
AG24	ENET_TXC	ETH_TXCLK	33	RGMII transmit clock
AG26	ENET_TD0	ETH_TXD0	34	RGMII transmit data 0
AF26	ENET_TD1	ETH_TXD1	35	RGMII transmit data 1
AG25	ENET_TD2	ETH_TXD2	36	RGMII transmit data 2
AF25	ENET_TD3	ETH_TXD3	37	RGMII transmit data 3
AF24	ENET_TX_CTL	ETH_TXEN	32	RGMII transmit enable
AE26	ENET_RXC	ETH_RXCLK	31	RGMII receive clock
AE27	ENET_RD0	ETH_RXD0	29	RGMII receive data 0
AD27	ENET_RD1	ETH_RXD1	28	RGMII receive data 1
AD26	ENET_RD2	ETH_RXD2	26	RGMII receive data 2
AC26	ENET_RD3	ETH_RXD3	25	RGMII receive data 3
AF27	ENET_RX_CTL	ETH_RXDV	30	RGMII receive data valid
AC27	ENET_MDC	MDC	40	Management data clock reference
AB27	ENET_MDIO	MDIO	39	Management data
R23	SD1_RESET_B	ENET_nRST	1	System reset
R24	SD1_STROBE	ENET_nINT	20	Ethernet interrupt output
N24	ENET_PWR_EN	ENET_PWR_EN	3	Ethernet Power enable

3.7. JTAG

The FLEX-IMX8M-Mini has an on module JTAG Controller that provides debug and test control with maximum security. The test access port is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M4 and Cortex A53 Cores DAP - debug access port.

For additional details, please refer to the “i.MX8M Mini Applications Processor Reference Manual”.

Figure 8 – FLEX-IMX8M-Mini JTAG Connector

NOTE : Pin 1 is far most thru-hole. Pin 8 is closest to the Wi-Fi / Bluetooth interface.

Table 8 - JTAG Signal Description

PIN	CPU BALL	Description
1	3V3	VDD_3V3 Signal
2	C27	JTAG_nTRST
3	F27	JTAG_TMS
4	E27	JTAG_TDI
5	E26	JTAG_TDO
6	NC	Not Connected
7	F26	JTAG_TCK
8	GND	Ground Signal

4. FLEX Compute Module Pin Assignment

Figure 9 – FLEX-IMX8M-Mini Board-to-Board Connectors

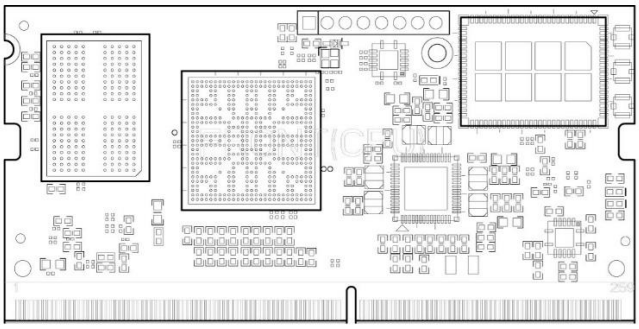


Table 9 – FLEX Compute Module Pin Assignment

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
1			VSYS	5V0	P	System input power (4.75 to 5.25V)
2			VSYS	5V0	P	System input power (4.75 to 5.25V)
3			VSYS	5V0	P	System input power (4.75 to 5.25V)
4			VSYS	5V0	P	System input power (4.75 to 5.25V)
5			VSYS	5V0	P	System input power (4.75 to 5.25V)
6			VSYS	5V0	P	System input power (4.75 to 5.25V)
7			3V3_REF	3V3	P	3.3V Reference Voltage for I/O
8			3V3_VDD	3V3	P	3.3V Output Voltage
9			SYS_nRST	1V8	I	Power Reset pin connected to PMIC
10			GND		P	Ground
11			GND		P	Ground
12	AR8035 pin 9		GBE_MDI0+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
13	AR8035 pin 15		GBE_MDI2+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal
14	AR8035 pin 10		GBE_MDI0-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
15	AR8035 pin 16		GBE_MDI2-	2V5	I/O	Gigabit Ethernet Media Dependent

					Interface (MDI) differential pair 2 negative signal
16			GND		P	Ground
17			GND		P	Ground
18	AR8035 pin 12		GBE_MDI1+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
19	AR8035 pin 18		GBE_MDI3+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
20	AR8035 pin 13		GBE_MDI1-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal
21	AR8035 pin 19		GBE_MDI3-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
22			GND		P	Ground
23			GND		P	Ground
24	AR8035 pin 24		LED1_nLink100	2V5	O	Gigabit Ethernet 100Mbit/sec LED link indicator
25	AR8035 pin 21		LED1_ACT	2V5	O	Gigabit Ethernet LED Activity indicator
26	AR8035 pin 22		LED1_nLink1000	2V5	O	Gigabit Ethernet 1000Mbit/sec LED link indicator
27	AR8035 pin 21		LED1_ACT_GND	GND	O	Gigabit Ethernet LED Activity indicator Ground Pin
28			GND		P	Ground
29			GND		P	Ground
30			NC			Not Connected
31	A9	MIPI_DSI_D0_N	MIPI_DSI_D0_N	1V8	O	MIPI Display Serial Interface data pair 0 negative signal
32			NC			Not Connected
33	B9	MIPI_DSI_D0_P	MIPI_DSI_D0_P	1V8	O	MIPI Display Serial Interface data pair 0 positive signal
34			GND		P	Ground
35			GND		P	Ground
36			NC			Not Connected
37	A10	MIPI_DSI_D1_N	MIPI_DSI_D1_N	1V8	O	MIPI Display Serial Interface data pair 1 negative signal
38			NC			Not Connected
39	B10	MIPI_DSI_D1_P	MIPI_DSI_D1_P	1V8	O	MIPI Display Serial Interface data pair 1 positive signal
40			GND		P	Ground

41			GND		P	Ground
42			NC			Not Connected
43	A12	MIPI_DSI_D2_N	MIPI_DSI_D2_N	1V8	O	MIPI Display Serial Interface data pair 2 negative signal
44			NC			Not Connected
45	B12	MIPI_DSI_D2_P	MIPI_DSI_D2_P	1V8	O	MIPI Display Serial Interface data pair 2 positive signal
46			GND		P	Ground
47			GND		P	Ground
48			NC			Not Connected
49	A13	MIPI_DSI_D3_N	MIPI_DSI_D3_N	1V8	O	MIPI Display Serial Interface data pair 3 negative signal
50			NC			Not Connected
51	B13	MIPI_DSI_D3_P	MIPI_DSI_D3_P	1V8	O	MIPI Display Serial Interface data pair 3 positive signal
52			GND		P	Ground
53			GND		P	Ground
54			NC			Not Connected
55	A11	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N	1V8	O	MIPI Display Serial Interface clock pair negative signal
56			NC			Not Connected
57	B11	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	1V8	O	MIPI Display Serial Interface clock pair positive signal
58			GND		P	Ground
59			GND		P	Ground
60			NC			Not Connected
61	AF8	SPDIF_EXT_CLK	PWM1_OUT	3V3	O	General Purpose Input Output with PWM control for MIPI DSI Brightness Control (DSI_BL_PWM)
62			NC			Not Connected
63	AD10	GPIO1_IO10	GPIO1_IO10	3V3	I/O	General Purpose Input Output MIPI DSI Display enable signal (DSI_EN)
64			NC			Not Connected
65	AC10	GPIO1_IO11	GPIO1_IO11	3V3	I/O	General Purpose Input Output MIPI DSI Display reset signal (DSI_RST)
66			NC			Not Connected
67	AB10	GPIO1_IO12	GPIO1_IO12	3V3	I/O	General Purpose Input Output MIPI DSI Display power enable (DSI_VDDEN)
68			GND		P	Ground
69			GND		P	Ground
70	A16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N	1V8	O	MIPI Camera Serial Interface clock pair negative signal
71			NC			Not Connected

72	B16	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	1V8	O	MIPI Camera Serial Interface clock pair positive signal
73			NC			Not Connected
74			GND		P	Ground
75			GND		P	Ground
76	A14	MIPI_CSI_D0_N	MIPI_CSI_D0_N	1V8	I	MIPI Camera Serial Interface data pair 0 negative signal
77			NC			Not Connected
78	B14	MIPI_CSI_D0_P	MIPI_CSI_D0_P	1V8	I	MIPI Camera Serial Interface data pair 0 positive signal
79			NC			Not Connected
80			GND		P	Ground
81			GND		P	Ground
82	A15	MIPI_CSI_D1_N	MIPI_CSI_D1_N	1V8	I	MIPI Camera Serial Interface data pair 1 negative signal
83			NC			Not Connected
84	B15	MIPI_CSI_D1_P	MIPI_CSI_D1_P	1V8	I	MIPI Camera Serial Interface data pair 1 positive signal
85			NC			Not Connected
86			GND		P	Ground
87			GND		P	Ground
88	A17	MIPI_CSI_D2_N	MIPI_CSI_D2_N	1V8	I	MIPI Camera Serial Interface data pair 2 negative signal
89			NC			Not Connected
90	B17	MIPI_CSI_D2_P	MIPI_CSI_D2_P	1V8	I	MIPI Camera Serial Interface data pair 2 positive signal
91			NC			Not Connected
92			GND		P	Ground
93			GND		P	Ground
94	A18	MIPI_CSI_D3_N	MIPI_CSI_D3_N	1V8	I	MIPI Camera Serial Interface data pair 3 negative signal
95			NC			Not Connected
96	B18	MIPI_CSI_D3_P	MIPI_CSI_D3_P	1V8	I	MIPI Camera Serial Interface data pair 3 positive signal
97			NC			Not Connected
98			GND		P	Ground
99			GND		P	Ground
100	AF12	GPIO1_IO05	GPIO1_IO05	3V3	O	General Purpose Input Output for MIPI Camera reset (CSI_RST)
101			NC			Not Connected
102	AG11	GPIO1_IO06	GPIO1_IO06	3V3	O	General Purpose Input Output for MIPI Camera power down signal (CSI_PWR_DWN)
103			NC			Not Connected
104	AC9	GPIO1_IO14	CCM_CLKO1	3V3	O	MIPI Camera input clock

105			NC			Not Connected
106			GND		P	Ground
107			NC			Not Connected
108			NC			Not Connected
109	AF14	GPIO1_IO01	PWM1_OUT	3V3	I/O	General Purpose Input Output with PWM control
110			NC			Not Connected
111	AD9	GPIO1_IO13	PWM2_OUT	3V3	I/O	General Purpose Input Output with PWM control
112			GND		P	Ground
113	AF9	SPDIF_TX	PWM3_OUT	3V3	I/O	General Purpose Input Output with PWM control
114			NC			Not Connected
115	AB9	GPIO1_IO15	PWM4_OUT	3V3	I/O	General Purpose Input Output with PWM control
116			NC			Not Connected
117	AG7	SAI3_RXC	GPIO4_IO29	3V3	I	PCI Express reset signal
118			GND		P	Ground
119	AC19	SAI2_RXFS	GPIO4_IO21	3V3	I	PCI Express Wake Signal
120			NC			Not Connected
121	AB22	SAI2_RXC	GPIO4_IO22	3V3	I	PCI Express Clock Request Signal
122			NC			Not Connected
123			NC			Not Connected
124			GND		P	Ground
125			NC			Not Connected
126			NC			Not Connected
127			GND		P	Ground
128			NC			Not Connected
129	A21	PCIE_CLK_N	PCIE_CLK_N	1V8	O	PCI Express clock differential pair negative signal
130			GND		P	Ground
131	B21	PCIE_CLK_P	PCIE_CLK_P	1V8	O	PCI Express clock differential pair positive signal
132			NC			Not Connected
133			GND		P	Ground
134			NC			Not Connected
135	A20	PCIE_TXN_N	PCIE_TXN_N	1V8	O	PCI Express Receive input differential pair negative signal
136			GND		P	Ground
137	B20	PCIE_TXN_P	PCIE_TXN_P	1V8	O	PCI Express Receive input differential pair positive signal
138			NC			Not Connected
139			GND		P	Ground
140			NC			Not Connected
141	A19	PCIE_RXN_N	PCIE_RXN_N	1V8	I	PCI Express Receive input differential pair negative signal
142			GND		P	Ground

143	B19	PCIE_RXN_P	PCIE_RXN_P	1V8	I	PCI Express Receive input differential pair positive signal
144			NC			Not Connected
145			NC			Not Connected
146			GND		P	Ground
147			NC			Not Connected
148			NC			Not Connected
149			GND		P	Ground
150			NC			Not Connected
151			NC			Not Connected
152			GND		P	Ground
153			NC			Not Connected
154			NC			Not Connected
155			GND		P	Ground
156			NC			Not Connected
157			NC			Not Connected
158			GND		P	Ground
159			NC			Not Connected
160	A22	USB1_DN	USB1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
161			GND		P	Ground
162	B22	USB1_DP	USB1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
163			NC			Not Connected
164			GND		P	Ground
165			NC			Not Connected
166	K23	NAND_DATA02	GPIO3_IO08	3V3	I/O	General Purpose Input Output for USB Over Current Detection
167			GND		P	Ground
168	F22	USB1_VBUS	USB1_VBUS	5V	I/O	Universal Serial Bus power
169	B8	ECSPI2_MOSI	ECSPI2_MOSI	3V3	O	Serial Peripheral Interface master output slave input signal.
170	D22	USB1_ID	USB1_ID	3V3	I	USB OTG ID Pin
171	A8	ECSPI2_MISO	ECSPI2_MISO	3V3	I/O	Serial Peripheral Interface master input slave output signal
172	AF10	GPIO1_IO09	USDHC3_RESET_B	3V3	O	Universal Serial Bus power enable
173	E6	ECSPI2_SCLK	ECSPI2_SCLK	3V3	O	Serial Peripheral Interface clock signal
174			NC			Not Connected
175	A6	ECSPI2_SS0	ECSPI2_SS0	3V3	O	Serial Peripheral Interface Chip Select 0 Signal
176	AF11	GPIO1_IO07	GPIO1_IO07	3V3	I/O	General Purpose Input Output for USB hub reset
177			NC			Not Connected
178	F23	USB2_VBUS	USB2_VBUS	5V	I	Universal Serial Bus power
179			GND		P	Ground

180			GND		P	Ground
181			NC			Not Connected
182			NC			Not Connected
183			NC			Not Connected
184			NC			Not Connected
185			NC			Not Connected
186			GND		P	Ground
187			NC			Not Connected
188			NC			Not Connected
189			NC			Not Connected
190			NC			Not Connected
191			GND		P	Ground
192			GND		P	Ground
193	E9	I2C1_SCL	I2C1_SCL	3V3	O	I2C bus clock line
194	A23	USB2_DN	USB2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
195	F9	I2C1_SDA	I2C1_SDA	3V3	I/O	I2C bus data line
196	B23	USB2_DP	USB2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
197	D10	I2C2_SCL	I2C2_SCL	3V3	O	I2C bus clock line
198			GND		P	Ground
199	D9	I2C2_SDA	I2C2_SDA	3V3	I/O	I2C bus data line
200	AF7	SAI3_RXD	SAI3_RXD	3V3	I	Integrated Interchip Sound (I2S) channel receive data line
201	E10	I2C3_SCL	I2C3_SCL	3V3	O	I2C bus clock line
202	AC6	SAI3_TXFS	SAI3_TXFS	3V3	O	Integrated Interchip Sound (I2S) channel frame synchronization signal
203	F10	I2C3_SDA	I2C3_SDA	3V3	I/O	I2C bus data line
204	AF6	SAI3_TXD	SAI3_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
205			NC			Not Connected
206	AG6	SAI3_TXC	SAI3_TXC	3V3	O	Integrated Interchip Sound (I2S) channel word clock signal
207			NC			Not Connected
208	AD6	SAI3_MCLK	SAI3_MCLK	3V3	O	Integrated Interchip Sound (I2S) channel master clock signal
209			GND		P	Ground
210			GND		P	Ground
211	AC24	SAI2_RXD0	SAI2_RXD	3V3	I	Integrated Interchip Sound (I^2S) channel receive data line
212	B7	ECSPI1_MOSI	UART3_TXD	3V3	O	Universal Asynchronous Receive Transmit transmit data signal
213	AD23	SAI2_TXFS	SAI2_TXFS	3V3	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal

214	D6	ECSPI1_SCLK	UART3_RXD	3V3	I	Universal Asynchronous Receive Transmit receive data signal
215	AC22	SAI2_TXD0	SAI2_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
216	B6	ECSPI1_SS0	UART3_RTS_B	3V3	O	Universal Asynchronous Receive Transmit request to send signal
217	AD22	SAI2_TXC	SAI2_TXC	3V3	O	Integrated Interchip Sound (I^2S) channel word clock signal
218	A7	ECSPI1_MISO	UART3_CTS_B	3V3	O	Universal Asynchronous Receive Transmit clear to send signal
219	AD19	SAI2_MCLK	SAI2_MCLK	3V3	O	Integrated Interchip Sound (I2S) channel master clock signal
220			GND		P	Ground
221			GND		P	Ground
222			NC			Not Connected
223	W23	SD2_CLK	USDHC2_CLK	1V8/ 3V3	O	MMC/SDIO Clock
224			NC			Not Connected
225	W24	SD2_CMD	USDHC2_CMD	1V8/ 3V3	I/O	MMC/SDIO Command
226			NC			Not Connected
227	AB23	SD2_DATA0	USDHC2_DATA0	1V8/ 3V3	IO	MMC/SDIO Data bit 0
228			NC			Not Connected
229	AB24	SD2_DATA1	USDHC2_DATA1	1V8/ 3V3	I/O	MMC/SDIO Data bit 1
230	V22	NVCC_SD2	NVCC_SD2	1V8/ 3V3	I/O	SD Card 2 power supply
231	V24	SD2_DATA2	USDHC2_DATA2	1V8/ 3V3	I/O	MMC/SDIO Data bit 2
232	AB26	SD2_RESET_B	SD2_RESET_B	3V3	O	SD Card 2 Reset Signal
233	V23	SD2_DATA3	USDHC2_DATA3	1V8/ 3V3	I/O	MMC/SDIO Data bit 3
234			GND		P	Ground
235	AA26	SD2_CD_B	USDHC2_CD_B	1V8/ 3V3	I	SD Card detect input (Active low)
236	A25	ONOFF	ONOFF	3V3	I	Power ON button input signal (Recommended to keep floating)
237			GND		P	Ground
238	AG13	GPIO1_IO02	WDOG1_B	3V3	I	Connected to the WDOG_B signal of PMIC and i.MX8M-Mini
239	E15	UART2_TXD	UART2_TXD	3V3	O	Universal Asynchronous

						Receive Transmit transmit data signal
240	AC15	SAI5_RXC	GPIO3_IO20	3V3	I/O	General Purpose Input Output
241	F15	UART2_RXD	UART2_RXD	3V3	I	Universal Asynchronous Receive Transmit receive data signal
242	P23	NAND_DATA00	GPIO3_IO06	3V3	I/O	General Purpose Input Output
243	F18	UART4_TXD	UART2_RTS_B	3V3	O	Universal Asynchronous Receive Transmit request to send signal
244	AG8	SAI3_RXFS	GPIO4_IO28	3V3	I/O	General Purpose Input Output
245	F19	UART4_RXD	UART2_CTS_B	3V3	O	Universal Asynchronous Receive Transmit clear to send signal
246	N23	NAND_DATA03	GPIO3_IO09	3V3	I/O	General Purpose Input Output
247			GND		P	Ground
248	AC13	SAI5_RXD3	GPIO3_IO24	3V3	I/O	General Purpose Input Output
249	BOOT SELECT PIN					
250	AD15	SAI5_MCLK	GPIO3_IO25	3V3	I/O	General Purpose Input Output
251	BOOT SELECT PIN					
252	AB15	SAI5_RXFS	GPIO3_IO19	3V3	I/O	General Purpose Input Output
253	BOOT SELECT PIN					
254	AG9	SPDIF_RX	GPIO5_IO04	3V3	I/O	General Purpose Input Output
255	BOOT SELECT PIN					
256	AB18	SAI1_MCLK	GPIO4_IO20	3V3	I/O	General Purpose Input Output
257	AG16	SAI1_RXFS	GPIO4_IO00	3V3	I/O	I2C bus data line for Bit Bang operation
258	AG10	GPIO1_IO08	GPIO1_IO08	3V3	I/O	General Purpose Input Output
259	AF16	SAI1_RXC	GPIO4_IO01	3V3	I/O	I2C bus clock line for Bit Bang operation
260			NC			Not Connected

5. FLEX-IMX8M-Mini External Interfaces

5.1. Ethernet

The FLEX-IMX8M-Mini provides a 10/100/1000-Mbit/s MAC ethernet interface which, implements layer 3 network acceleration functions. These functions are designed to accelerate the processing of various common networking protocols, such as IP, TCP, UDP, and ICMP, providing wire speed services to client applications.

The Ethernet interface provides following features.

- Triple speed 10/100/1000 Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard.
- The MAC layer provides compatibility with half- or full-duplex 10/100 Mbit/s Ethernet LANs and full-duplex gigabit Ethernet LANs.

For additional details, please refer to the “Ethernet MAC (ENET)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 10 - Ethernet Signal Description

PIN	IC Pin	Signal	V	I/O	Description
12	AR8035 pin 9	GBE_MDI0+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
13	AR8035 pin 15	GBE_MDI2+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal
14	AR8035 pin 10	GBE_MDI0-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
15	AR8035 pin 16	GBE_MDI2-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal
18	AR8035 pin 12	GBE_MDI1+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
19	AR8035 pin 18	GBE_MDI3+	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
20	AR8035 pin 13	GBE_MDI1-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal
21	AR8035 pin 19	GBE_MDI3-	2V5	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
24	AR8035 pin 24	LED1_nLink100	2V5	O	Gigabit Ethernet 100Mbit/sec LED link indicator
25	AR8035 pin 21	LED1_ACT	2V5	O	Gigabit Ethernet LED Activity indicator
26	AR8035 pin 22	LED1_nLink1000	2V5	O	Gigabit Ethernet 1000Mbit/sec LED link indicator
27	AR8035 pin 21	LED1_ACT_GND	GND	O	Gigabit Ethernet LED Activity indicator Ground Pin

5.2. MIPI Display

The Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

Key features of the MIPI DSI Controller Core include:

- Implements all three DSI Layers (Pixel to Byte packing, Low Level Protocol, Lane Management)
- Support for Command and Video Modes
- Host Version
- Scalable data lane support, 1 to 4 Data Lanes
- Optional bidirectional support on lane 0
- Supports High Speed and Low Power operation
- Support for all DSI data types and formats
- Virtual Channel support
- Supports ULPS mode
- Full Low-Level Protocol Error and Contention detection and reporting
- Supports continuous and non-continuous Clock Lane operation
- Supports multiple packets per transmission
- Support for all three Video Mode packet sequences
    - Non-Burst Mode with Sync Pulses
    - Non-Burst Mode with Sync Events
    - Burst mode
- Support for bus turnaround signaling
- Flexible packet based user interface
- APB interface option (status and control)
- Display Pixel Interface Core (DPI-2) option
- Display Bus Interface Core (DBI-2) option
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant

For additional details, please refer to the “MIPI DSI Host Controller (MIPI_DSI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 11 - MIPI Display Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
31	A9	MIPI_DSI_D0_N	MIPI_DSI_D0_N	1V8	O	MIPI Display Serial Interface data pair 0 negative signal
33	B9	MIPI_DSI_D0_P	MIPI_DSI_D0_P	1V8	O	MIPI Display Serial Interface data pair 0 positive signal
37	A10	MIPI_DSI_D1_N	MIPI_DSI_D1_N	1V8	O	MIPI Display Serial Interface data pair 1 negative signal
39	B10	MIPI_DSI_D1_P	MIPI_DSI_D1_P	1V8	O	MIPI Display Serial Interface data pair 1 positive signal
43	A12	MIPI_DSI_D2_N	MIPI_DSI_D2_N	1V8	O	MIPI Display Serial Interface data pair 2 negative signal
45	B12	MIPI_DSI_D2_P	MIPI_DSI_D2_P	1V8	O	MIPI Display Serial Interface data pair 2 positive signal
49	A13	MIPI_DSI_D3_N	MIPI_DSI_D3_N	1V8	O	MIPI Display Serial Interface data pair 3 negative signal
51	B13	MIPI_DSI_D3_P	MIPI_DSI_D3_P	1V8	O	MIPI Display Serial Interface data pair 3 positive signal
55	A11	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N	1V8	O	MIPI Display Serial Interface clock pair negative signal
57	B11	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	1V8	O	MIPI Display Serial Interface clock pair positive signal
61	AF8	SPDIF_EXT_CLK	PWM1_OUT	3V3	O	General Purpose Input Output with PWM control for MIPI DSI Brightness Control (DSI_BL_PWM)
63	AD10	GPIO1_IO10	GPIO1_IO10	3V3	I/O	General Purpose Input Output MIPI DSI Display enable signal (DSI_EN)
65	AC10	GPIO1_IO11	GPIO1_IO11	3V3	I/O	General Purpose Input Output MIPI DSI Display reset signal (DSI_RST)
67	AB10	GPIO1_IO12	GPIO1_IO12	3V3	I/O	General Purpose Input Output MIPI DSI Display power enable (DSI_VDDEN)

5.3. MIPI Camera

This section introduces the MIPI CSI-2 RX subsystem with the CSI-2 RX PHY and host controller. This subsystem handles the sensor/image input and process for all the input imaging devices.

The MIPI-CSI2 Controller has the following key features:

- Implements all three CSI-2 MIPI layers (Pixel to byte packing, low level protocol,
- Lane management)
- Supports unidirectional Master operation
- Transmitter and receiver versions
- Scalable data lane support, 1 to 4 Data Lanes
- Supports high speed mode(80Mbps - 1.5Gbps) per lane, providing 4K@30fps capability for the 4 lanes
- Supports 10Mbps data rate in low power mode
- Includes high speed deserializers
- Loopback testability support
- Support for all CSI-2 data types
- Virtual Channel support
- Support for DPHY Ultra Low Power State (ULPS)
- Error collection support (Rx Only)
- Flexible pixel-based user interface
- Supports user generated packets
- Supports single, double, or quad pixel interface
- Supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs
- Delivered fully integrate and verified with target MIPI D-PHY
- RX Video Interface
- APB Control and Status Register (CSR) interface with IRQ support

For additional details, please refer to the “MIPI CSI Host Controller (MIPI_CSI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 12 - MIPI Camera Control Signals

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
70	A16	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N	1V8	O	MIPI Camera Serial Interface clock pair negative signal
72	B16	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	1V8	O	MIPI Camera Serial Interface clock pair positive signal
76	A14	MIPI_CSI_D0_N	MIPI_CSI_D0_N	1V8	I	MIPI Camera Serial Interface data pair 0 negative signal
78	B14	MIPI_CSI_D0_P	MIPI_CSI_D0_P	1V8	I	MIPI Camera Serial Interface data pair 0 positive signal
82	A15	MIPI_CSI_D1_N	MIPI_CSI_D1_N	1V8	I	MIPI Camera Serial Interface data pair 1 negative signal
84	B15	MIPI_CSI_D1_P	MIPI_CSI_D1_P	1V8	I	MIPI Camera Serial Interface data pair 1 positive signal
88	A17	MIPI_CSI_D2_N	MIPI_CSI_D2_N	1V8	I	MIPI Camera Serial Interface data pair 2 negative signal
90	B17	MIPI_CSI_D2_P	MIPI_CSI_D2_P	1V8	I	MIPI Camera Serial Interface data pair 2 positive signal
94	A18	MIPI_CSI_D3_N	MIPI_CSI_D3_N	1V8	I	MIPI Camera Serial Interface data pair 3 negative signal
96	B18	MIPI_CSI_D3_P	MIPI_CSI_D3_P	1V8	I	MIPI Camera Serial Interface data pair 3 positive signal
100	AF12	GPIO1_IO05	GPIO1_IO05	3V3	O	General Purpose Input Output for MIPI Camera reset (CSI_RST)
102	AG11	GPIO1_IO06	GPIO1_IO06	3V3	O	General Purpose Input Output for MIPI Camera power down signal (CSI_PWR_DWN)
104	AC9	GPIO1_IO14	CCM_CLKO1	3V3	O	MIPI Camera input clock

5.4. Audio Interface

The FLEX-IMX8M-Mini provides multiple I²S (or I²S) interfaces that support fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

The I²S Interface supports the following features:

- Transmitter with independent bit clock and frame sync supporting 1 data line
- Receiver with independent bit clock and frame sync supporting 1 data line
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 128 × 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word

For additional details, please refer to the “Synchronous Audio Interface (SAI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 13 - I2S-1 Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
200	AF7	SAI3_RXD	SAI3_RXD	3V3	I	Integrated Interchip Sound (I2S) channel receive data line
202	AC6	SAI3_TXFS	SAI3_TXFS	3V3	O	Integrated Interchip Sound (I2S) channel frame synchronization signal
204	AF6	SAI3_TXD	SAI3_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
206	AG6	SAI3_TXC	SAI3_TXC	3V3	O	Integrated Interchip Sound (I2S) channel word clock signal
208	AD6	SAI3_MCLK	SAI3_MCLK	3V3	O	Integrated Interchip Sound (I2S) channel master clock signal

Table 14 - I2S-2 Audio Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
211	AC24	SAI2_RXD0	SAI2_RXD	3V3	I	Integrated Interchip Sound (I^2S) channel receive data line
213	AD23	SAI2_TXFS	SAI2_TXFS	3V3	O	Integrated Interchip Sound (I^2S) channel frame synchronization signal
215	AC22	SAI2_TXD0	SAI2_TXD	3V3	O	Integrated Interchip Sound (I2S) channel transmit data line
217	AD22	SAI2_TXC	SAI2_TXC	3V3	O	Integrated Interchip Sound (I^2S) channel word clock signal
219	AD19	SAI2_MCLK	SAI2_MCLK	3V3	O	Integrated Interchip Sound (I2S) channel master clock signal

5.5. PCI Express

This block provides information regarding PCIe PHY and its features. PCIe PHY supports 6.0 Gbps data rate and complies to PCI Express base specification 2.1. The functions that are performed by the transceiver include serializing the 8B/10B encoded data for transmission, de-serializing received code groups, and word alignment.

When transmitting, the transceiver accepts two or four 10-bit 8B/10B encoded transmit characters, latches them and serializes the data onto the PCIE_TX_P/PCIE_TX_N differential outputs at 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps. It also performs 8B/10B encoding for 8-bit data from the PIPE interface.

When receiving, the transceiver also samples received serial data on the PCIE_RX_P / PCIE_RX_N differential inputs, deserializes it into two or four 10-bit received characters and detects the K28.5 character (0011111010 or 1100000101) for word alignment. It also applies 8B/10B decoding for 8-bit data to the PIPE interface. PCIe PHY core contains on-chip PLL circuitry for synthesis of the baud-rate transmitting clocks, and extraction of the retimed clocks from the received serial stream.

The following list the key features of the PCIe PHY:

- 1.5 / 2.5 / 3.0 / 5.0 / 6.0 Gbps Serializer / Deserializer
- Compliant with PCI Express Base Specification 2.1
- Compliant with PIPE Specification 2.0
- 8 / 16 / 20 / 40-bit CMOS Interface for Transmitter and Receiver
- 25 / 100 MHz Reference Clock
- K28.5 Detection for Word Alignment
- 8B/10B Encoding / Decoding
- Receiver Detection
- Supports Spread Spectrum Clocking in Transmitter and Receiver

For additional details, please refer to the “PCI Express (PCIe)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 15 - PCI Express Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
117	AG7	SAI3_RXC	GPIO4_IO29	3V3	I	PCI Express reset signal
119	AC19	SAI2_RXFS	GPIO4_IO21	3V3	I	PCI Express Wake Signal
121	AB22	SAI2_RXC	GPIO4_IO22	3V3	I	PCI Express Clock Request Signal
129	A21	PCIE_CLK_N	PCIE_CLK_N	1V8	O	PCI Express clock differential pair negative signal
131	B21	PCIE_CLK_P	PCIE_CLK_P	1V8	O	PCI Express clock differential pair positive signal
135	A20	PCIE_TXN_N	PCIE_TXN_N	1V8	O	PCI Express Receive input differential pair negative signal
137	B20	PCIE_TXN_P	PCIE_TXN_P	1V8	O	PCI Express Receive input differential pair positive signal
141	A19	PCIE_RXN_N	PCIE_RXN_N	1V8	I	PCI Express Receive input differential pair negative signal
143	B19	PCIE_RXN_P	PCIE_RXN_P	1V8	I	PCI Express Receive input differential pair positive signal

NOTE: The PCIE_TX pair has decoupling capacitors on the FLEX Compute Module valued 10nF

5.6. Universal Serial Bus (USB) Interface

The FLEX-IMX8M-Mini incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:
USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Support charger detection

USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to the “Universal Serial Bus Controller (USB)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 16 - USB Host Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
172	AF10	GPIO1_IO09	USDHC3_RESET_B	3V3	O	Universal Serial Bus power enable
176	AF11	GPIO1_IO07	GPIO1_IO07	3V3	I/O	General Purpose Input Output for USB hub reset
178	F23	USB2_VBUS	USB2_VBUS	5V	I	Universal Serial Bus power
194	A23	USB2_DN	USB2_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
196	B23	USB2_DP	USB2_DP	3V3	I/O	Universal Serial Bus differential pair positive signal

Table 17 - USB OTG Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
160	A22	USB1_DN	USB1_DN	3V3	I/O	Universal Serial Bus differential pair negative signal
162	B22	USB1_DP	USB1_DP	3V3	I/O	Universal Serial Bus differential pair positive signal
166	K23	NAND_DATA02	GPIO3_IO08	3V3	I/O	General Purpose Input Output for USB Over Current Detection
168	F22	USB1_VBUS	USB1_VBUS	5V	I/O	Universal Serial Bus power
170	D22	USB1_ID	USB1_ID	3V3	I	USB OTG ID Pin

NOTE: While using USB OTG in USB HOST mode. The USB_ID pin should have a pull-down resistor to GND.

5.7. SDIO/MMC Interface

The FLEX-IMX8M-Mini features a MMC / SD / SDIO host interfaces connected to the NXP i.MX8M Mini integrated “Ultra Secured Digital Host Controller” (uSDHC).

The following main features are supported by uSDHC:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, MiniSD Memory, SDIO, MiniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 208 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to the “Ultra Secured Digital Host Controller (uSDHC)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 18 - SDIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
223	W23	SD2_CLK	USDHC2_CLK	1V8/ 3V3	O	MMC/SDIO Clock
225	W24	SD2_CMD	USDHC2_CMD	1V8/ 3V3	I/O	MMC/SDIO Command
227	AB23	SD2_DATA0	USDHC2_DATA0	1V8/ 3V3	IO	MMC/SDIO Data bit 0
229	AB24	SD2_DATA1	USDHC2_DATA1	1V8/ 3V3	I/O	MMC/SDIO Data bit 1
230	V22	NVCC_SD2	NVCC_SD2	1V8/ 3V3	I/O	SD Card 2 power supply
231	V24	SD2_DATA2	USDHC2_DATA2	1V8/ 3V3	I/O	MMC/SDIO Data bit 2
232	AB26	SD2_RESET_B	SD2_RESET_B	3V3	O	SD Card 2 Reset Signal
233	V23	SD2_DATA3	USDHC2_DATA3	1V8/ 3V3	I/O	MMC/SDIO Data bit 3
235	AA26	SD2_CD_B	USDHC2_CD_B	1V8/ 3V3	I	SD Card detect input (Active low)

5.8. Universal Asynchronous Receiver/Transmitter (UART) Interface

The FLEX-IMX8M-Mini Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

For additional details, please refer to the “Universal Asynchronous Receiver/Transmitter (UART)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 19 – UART3 Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
212	B7	ECSPI1_MOSI	UART3_TXD	3V3	O	Universal Asynchronous Receive Transmit transmit data signal
214	D6	ECSPI1_SCLK	UART3_RXD	3V3	I	Universal Asynchronous Receive Transmit receive data signal
216	B6	ECSPI1_SS0	UART3_RTS_B	3V3	O	Universal Asynchronous Receive Transmit request to send signal
218	A7	ECSPI1_MISO	UART3_CTS_B	3V3	O	Universal Asynchronous Receive Transmit clear to send signal

Table 20 – UART2 Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
239	E15	UART2_TXD	UART2_TXD	3V3	O	Universal Asynchronous Receive Transmit transmit data signal
241	F15	UART2_RXD	UART2_RXD	3V3	I	Universal Asynchronous Receive Transmit receive data signal
243	F18	UART4_TXD	UART2_RTS_B	3V3	O	Universal Asynchronous Receive Transmit request to send signal
245	F19	UART4_RXD	UART2_CTS_B	3V3	O	Universal Asynchronous Receive Transmit clear to send signal

NOTE: If you need a third (3rd) UART you can dedicate PIN 243 and 245 to operate in UART4 mode

5.9. Serial Peripheral Interface (SPI)

The FLEX-IMX8M-Mini has an onboard SPI interface that can operate in either master or SPI slave mode.

The SPI Interface includes the following features:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

For additional details, please refer to the “Enhanced Configurable SPI (ECSPI)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 21 - SPI Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
169	B8	ECSPI2_MOSI	ECSPI2_MOSI	3V3	O	Serial Peripheral Interface master output slave input signal.
171	A8	ECSPI2_MISO	ECSPI2_MISO	3V3	I/O	Serial Peripheral Interface master input slave output signal
173	E6	ECSPI2_SCLK	ECSPI2_SCLK	3V3	O	Serial Peripheral Interface clock signal
175	A6	ECSPI2_SS0	ECSPI2_SS0	3V3	O	Serial Peripheral Interface Chip Select 0 Signal

5.10. I²C Bus

The FLEX-IMX8M-Mini incorporates several I²C interfaces. I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, Minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.
The following features are supported:

- Compliance with Philips I2C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to the "I²C Controller (I²C)" chapter of the "i.MX8M Mini Applications Processor Reference Manual".

Table 22 - I²C Bus Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
193	E9	I2C1_SCL	I2C1_SCL	3V3	O	I2C bus clock line
195	F9	I2C1_SDA	I2C1_SDA	3V3	I/O	I2C bus data line
197	D10	I2C2_SCL	I2C2_SCL	3V3	O	I2C bus clock line
199	D9	I2C2_SDA	I2C2_SDA	3V3	I/O	I2C bus data line
201	E10	I2C3_SCL	I2C3_SCL	3V3	O	I2C bus clock line
203	F10	I2C3_SDA	I2C3_SDA	3V3	I/O	I2C bus data line

NOTE: All I²C bus data and clock lines for all I²C interfaces have 4.7K Ω pull-up resistors present on the FLEX-IMX8M-Mini module.

5.10.1. I²C Bit Bang Interface

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
257	AG16	SAI1_RXFS	GPIO4_IO00	3V3	I/O	I2C bus data line for Bit Bang operation
259	AF16	SAI1_RXC	GPIO4_IO01	3V3	I/O	I2C bus clock line for Bit Bang operation

5.11. General Purpose Input / Output (GPIO)

The FLEX-IMX8M-Mini has 10 dedicated GPIO pins at 3.3V. Many of the other pins used on the FLEX Compute Module can be put in GPIO module however doing so might break scalability with other FLEX Compute Modules.
The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to the “General Purpose Input / Output (GPIO)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 23 - GPIO Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
240	AC15	SAI5_RXC	GPIO3_IO20	3V3	I/O	General Purpose Input Output
242	P23	NAND_DATA00	GPIO3_IO06	3V3	I/O	General Purpose Input Output
244	AG8	SAI3_RXFS	GPIO4_IO28	3V3	I/O	General Purpose Input Output
246	N23	NAND_DATA03	GPIO3_IO09	3V3	I/O	General Purpose Input Output
248	AC13	SAI5_RXD3	GPIO3_IO24	3V3	I/O	General Purpose Input Output
250	AD15	SAI5_MCLK	GPIO3_IO25	3V3	I/O	General Purpose Input Output
252	AB15	SAI5_RXFS	GPIO3_IO19	3V3	I/O	General Purpose Input Output
254	AG9	SPDIF_RX	GPIO5_IO04	3V3	I/O	General Purpose Input Output
256	AB18	SAI1_MCLK	GPIO4_IO20	3V3	I/O	General Purpose Input Output
258	AG10	GPIO1_IO08	GPIO1_IO08	3V3	I/O	General Purpose Input Output

5.12. Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

The FLEX-IMX8M-Mini has 4 dedicated PWM pins at 1.8V.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to Minimize interrupt overhead
- 12-bit pre-scaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

For additional details, please refer to the “Pulse Width Modulation (PWM)” chapter of the “i.MX8M Mini Applications Processor Reference Manual”.

Table 24 - PWM Signal Description

PIN	CPU BALL	CPU PAD NAME	Signal	V	I/O	Description
109	AF14	GPIO1_IO01	PWM1_OUT	3V3	I/O	General Purpose Input Output with PWM control
111	AD9	GPIO1_IO13	PWM2_OUT	3V3	I/O	General Purpose Input Output with PWM control
113	AF9	SPDIF_TX	PWM3_OUT	3V3	I/O	General Purpose Input Output with PWM control
115	AB9	GPIO1_IO15	PWM4_OUT	3V3	I/O	General Purpose Input Output with PWM control

NOTE: When using PWM1_OUT for MIPI DSI Brightness Control on connector PIN 61 is used. You can only use PIN 109 in GPIO mode to avoid conflicts.

5.13. Manufacturing and Boot Control

The FLEX-IMX8M-Mini has a number of pins to override the default boot media present on the FLEX-IMX8M-Mini Compute Module or enable debug serial loader functionality.

Table 25 - Boot Selection Pins

PIN	Description
249	BOOT SELECT PIN
251	BOOT SELECT PIN
253	BOOT SELECT PIN
255	BOOT SELECT PIN

5.13.1. eMMC Boot Mode

The FLEX-IMX8M-Mini Compute Module automatically boot from the internal eMMC if the all control signals keep floating or if the pins are connected as follow:

Table 25 – eMMC Boot Mode Configuration

PIN	Description
249	HIGH (3V3)
251	HIGH (3V3)
253	HIGH (3V3)
255	HIGH (3V3)

5.13.2. Serial Downloader Boot Mode

To boot the FLEX-IMX8M-Mini in Serial Download Mode. The boot signals need to be connected as

Table 26 - Serial Downloader Boot Mode Configuration

PIN	Description
249	Has no function while entering Serial Download Mode
251	Has no function while entering Serial Download Mode
253	LOW (GND)
255	LOW (GND)

NOTE : Pin 249 and Pin 251 are disregarded when Pin 253 and Pin 255 are set to perform Serial Downloader boot mode.

5.13.3. SD Card Boot Mode

To boot the FLEX-IMX8M-Mini from a SD card on the baseboard. The boot signals need to be connected as

Table 27 - SD Card Boot Mode Configuration

PIN	Description
249	LOW (GND)
251	LOW (GND)
253	HIGH (3V3)
255	HIGH (3V3)

5.14. Input Power Requirements

The FLEX-IMX8M-Mini is designed to be driven with a single input power rail.
The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VSYS pins should be connected to the main power source.

Table 28 - Input Power Signals

POWER Rail	Nominal Input	Input Range	Maximum Input Ripple
VSYS	5V	+4.75V to +5.25V	+/- 50mV

5.14.1. Reference and Output Power

The FLEX-IMX8M-Mini is a versatile system on module that can be incorporated in an embedded system where the carrier board will have additional requirements for 3.3V.

For this purpose the FLEX-IMX8M-Mini integrates a 3.3V reference voltage pin and an additional 3.3V power output.

Table 29 - Power Management Signals

PIN	Description
7	3.3V Reference Voltage for I/O
8	3.3V Output Voltage maximum 500mA

6. Ordering Information

TechNexion provides a complete product portfolio for the FLEX-IMX8M-Mini to assist our customers to evaluate, proto-type, integrate and mass produce solutions with our FLEX Compute Modules.

6.1. FLEX Compute Module Product Ordering Part Numbers

The FLEX-IMX8M-Mini is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

Standard part numbers can be easily found on the FLEX-IMX8M-Mini product page on the TechNexion corporate homepage.

6.2. Custom Part Number Rule

The FLEX-IMX8M-Mini can be ordered in custom tailored configuration to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry Minimum order quantities (MOQ). Please connect with your TechNexion distributor or account manager for conditions and availability.

Part number format: **FLEX-IMX8MMx-xx-Rxx-Exx-xxxx-xx-xxxx**

Interface	Code	Description
Processor	IMX8MMQ	NXP i.MX8M Mini Quad
Processor Speed	18	1.8Ghz
Memory	R10	1GB LPDDR4
	R20	2GB LPDDR4
	R40	4GB LPDDR4
Storage	E16	eMMC 16GB
	EXX	eMMC other capacity
Wi-Fi / Bluetooth	-	-
	9377	Qualcomm QCA9377 802.11a/b/g/n/ac (2.4 + 5GHz) + Bluetooth 5
Temperature Range	-	Commercial Temperature range (0° to +60° C) (Default)
	TE	Extended Temperature range (-20° to +70° C)
	TI	Industrial Temperature range (-40° to +85° C)
Custom ID	XXXX	Custom Part number ID for customized software loader and special component (BOM)

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TechNexion Ltd.
16F-5, No. 736, Zhongzheng Road,
ZhongHe District, 23511, New Taipei City, Taiwan
Phone : +886-2-82273585
Fax : +886-2-82273590
E-mail : sales@TechNexion.com
Web : https://www.TechNexion.com/